Sink/Source DDR Termination Regulator

DESCRIPTION

The EUP7998 is a high performance linear regulator designed to provide power for termination of a DDR memory bus. It significantly reduces parts count, board space and overall system cost over previous switching solutions.

The EUP7998 maintains a fast transient response using only 20µF or 30µF output capacitance. The EUP7998 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3 and Low Power DDR3/DDR4 VTT bus termination.

The EUP7998 provides current and thermal limits to prevent damage to the linear regulator. Additionally, The EUP7998 generates an open-drain PGOOD signal to monitor the output regulation. An active high enable pin EN can pull VTT low, but REFOUT will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

The EUP7998 is available in the 3mm × 3mm TDFN-10 and SOP-8 (EP) packages.

FEATURES

- VLDOIN Input Voltage Range: 1.1V to 3.5V
- VIN Input Voltage Range: 2.375V to 5.5V
- Typically 3×10µF MLCCs stable for DDR
- Fast Load-Transient Response
- ±10mA Buffered Reference (REFOUT)
- Meet DDR, DDR2 JEDEC Specifications. Supports DDR3 and Low-Power DDR3/DDR4 VTT Applications
- Power-Good Window Comparator
- With Soft Start, UVLO and OCP
- Thermal Shutdown
- Available in 10-Pin 3mm×3mm TDFN and SOP-8 (EP) packages
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- Notebook/Desktop/Server
- DDR Memory Termination
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box

Typical Application Circuit

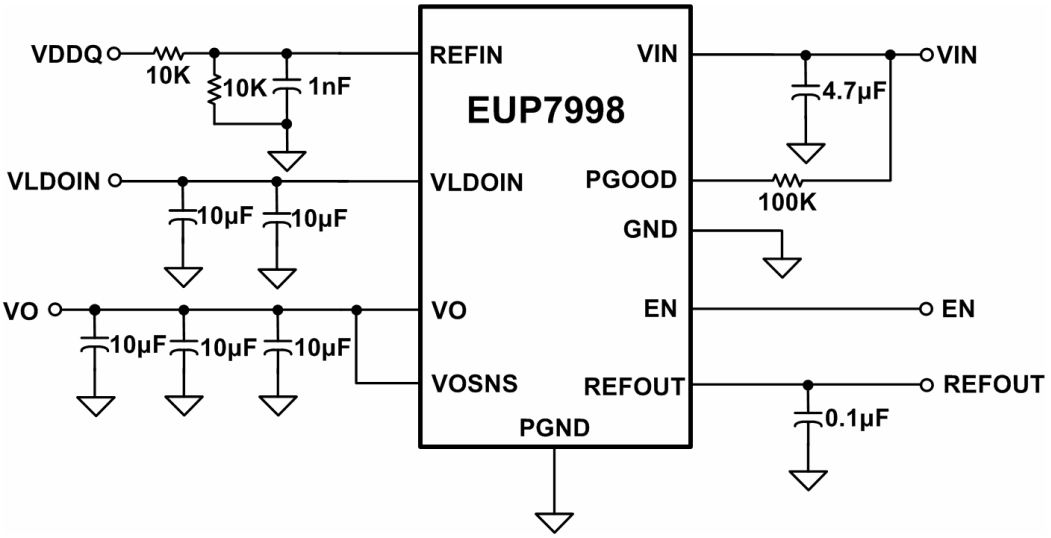


Figure 1. For TDFN-10 package

Typical Application Circuit (continued)

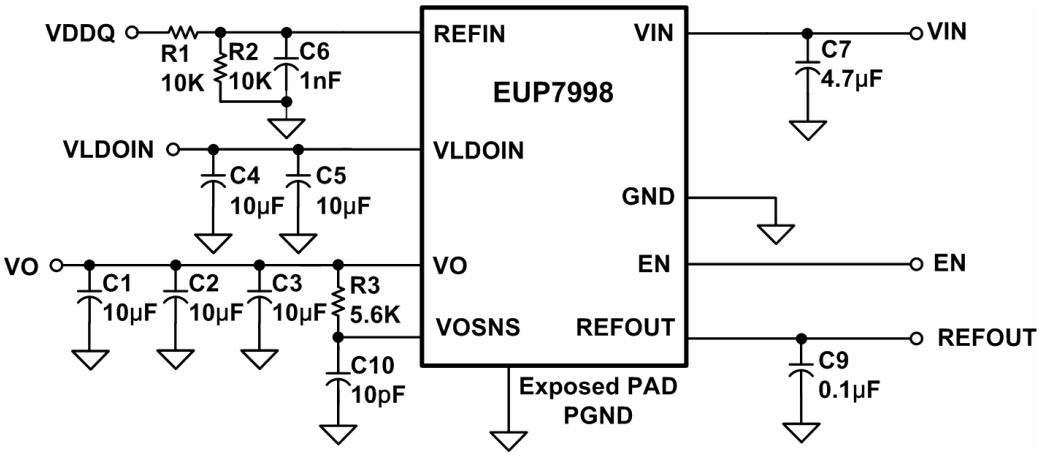
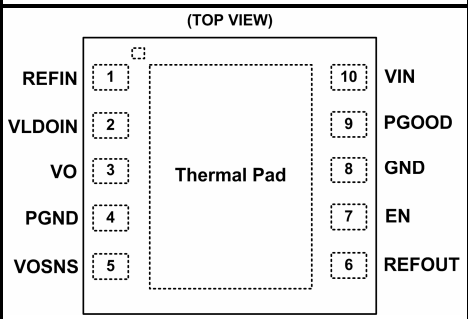
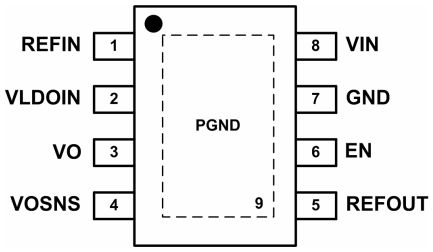


Figure 2. For SOP-8(EP) package

Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
TDFN-10		SOP-8 (EP)	

Pin Description

PIN	TDFN-10	SOP-8 (EP)	DESCRIPTION
REFIN	1	1	External Reference Input
VLDOIN	2	2	Power Supply of the LDO. Internally connected to the output source MOSFET.
VO	3	3	Output of the LDO
PGND	4	9 (Thermal pad)	Power Ground
VOSNS	5	4	Voltage sense input for the LDO. Connect to positive terminal of the output capacitor.
REFOUT	6	5	Buffered Reference Output. The output of the unity-gain reference input buffer sources and sinks over 10mA. Bypass REFOUT to GND with a 0.1µF ceramic capacitor.
EN	7	6	Enable Control Input. Active High Input. For DDR VTT application, connect EN to SLP_S3.
GND	8	7	Ground
PGOOD	9	-	Open-Drain Power-Good Output
VIN	10	8	Power Supply Input. Connect to the system supply voltage. Bypass VIN to GND with a 1µF or 4.7µF ceramic capacitor.

Note(1):PGND, GND and thermal pad must be connected together outside under thermal pad.